INTELLIGENT DISPLAY MODULE
SPECIFICATIONS

Datasheet Release 2016-02-11
for PLCD-35

Hardware Revision: 2h4
Firmware Revision: u3v1
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### About Variations

We work continuously to improve our products. Because display technologies are quickly evolving, these products may have component or process changes. Slight variations (for example, contrast, color, or intensity) between lots are normal. If you need the highest consistency, whenever possible, order and arrange delivery for your production runs at one time so your displays will be from the same lot.

### About Volatility

The display has nonvolatile memory.
INTRODUCTION

MAIN FEATURES PLCD-35

- Large easy-to-read display in a compact size can display 20 characters x 2 lines.
- Active Area is 63.55 (W) x 10.35 (H) millimeters.
- Display modules have a 12 o’clock viewing direction. See Optical Characteristics (Pg. 14).
- Temperature operating range is 0°C minimum to +50°C maximum.
- USB interface (factory default 115200 baud equivalent throughput).
- Integrated LED backlit 4-button translucent silicone keypad allows assignment of keys to be shown easily on the display. Fully decoded keypad: any key combination is valid and unique. See command 32: Key Legends (Pg. 47).
- Select from four colors of overlays.
- Backlight is fully voltage regulated over the power supply range. Adjustments to the backlight brightness can be made, although it is not necessary in most situations.
- The PLCD-35 has a RockWorks RW1067 controller.
- Robust packet based communications protocol with 16-bit CRC.
- ATX power supply control functionality allows the keypad buttons to replace the Power and Reset switches on your system, simplifying front panel design.
- Nonvolatile memory capability (EEPROM):
  - Customize the “power-on” display settings.
  - 16-byte “scratch” register for storing IP address, netmask, system serial number . . .
- Hardware watchdog can reset host system on host software failure.
- The PLCD-35 may be used with our optional PCBA (System Cooling Accessory Board) to add fan and temperature sensor and fan functions.
- Display is RoHS compliant.
- Supplier is ISO 9001:2008 certified.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>PLCD-35</th>
</tr>
</thead>
</table>
| LED Backlight | Display: white, 4 on 1 edge  
Keypad: blue |
| Fluid | STN |
| Glass Color | blue |
| Image | negative |
| Polarizer Film | transmissive |
| Viewing Angle | 12 o’clock |

Negative Image: Display can be read in typical office lighting and in dark areas. May be difficult to read in direct sunlight.

Viewing Angle: See Optical Characteristics (Pg. 14).
## PHYSICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>ITEM</th>
<th>SPECIFICATION</th>
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<tbody>
<tr>
<td><strong>Display Module Overall Dimensions</strong> (includes built-in bracket)</td>
<td></td>
</tr>
<tr>
<td>Width</td>
<td>101.60 (W) mm</td>
</tr>
<tr>
<td>Height</td>
<td>25.40 (H) mm</td>
</tr>
<tr>
<td>Depth</td>
<td>93.10 (D) mm (includes keypad)</td>
</tr>
<tr>
<td>Viewing Area</td>
<td>66.0 (W) x 13.8 (H) mm</td>
</tr>
<tr>
<td>Active Area</td>
<td>63.55 (W) x 10.35 (H) mm</td>
</tr>
<tr>
<td>Character Size (5 x 7)</td>
<td>2.60 (W) x 4.50 (H) mm</td>
</tr>
<tr>
<td>Character Pitch (6 x 8)</td>
<td>3.18 (W) x 5.20 (H) mm</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>0.53 (W) x 0.65 (H) mm</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>0.48 (W) x 0.60 (H) mm</td>
</tr>
<tr>
<td>Keystroke Travel (approximate)</td>
<td>~2.4 mm</td>
</tr>
<tr>
<td>Weight</td>
<td>80 grams (typical)</td>
</tr>
</tbody>
</table>
Top View PLCD-35 With Built-In Drive Bay Bracket

Front View PLCD-35 With Built-In Drive Bay Bracket

Side View PLCD-35 With Built-In Drive Bay Bracket

PLCD-35 Intelligent Display Module
Figure 2. PLCD-35 Back View, Character Details, And Pixel Details

5 x 7 Character
Black Outline

3.18
2.60

6 x 8 Matrix
Green Outline

4.50

Character Detail A

Pixel Detail B

5 x 7 Character
Black Outline

6 x 8 Matrix
Green Outline

5.20

Scale:
Units:
Drawing Number:
Hardware Rev.:
Sheet:

Part No.(s):
PLCD-35

Not to scale

2h4

2016-02-11
ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM

Figure 3. System Block Diagram
DUTY AND BIAS

The duty cycle, also known as duty ratio or multiplex rate, is the fraction of total frame time that each row of the display is addressed.

The drive bias, also known as voltage margin, is related to the number of voltage levels used when driving the display. Bias is defined as 1/(number of voltage levels-1). The more segments driven by each driver, the higher number of voltage levels are required. There is a direct relationship between the bias and the duty.

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
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<th>SYMBOL</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
</tr>
</thead>
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<tr>
<td>TOP</td>
<td>0°C</td>
<td>+50°C</td>
</tr>
<tr>
<td>TST</td>
<td>-10°C</td>
<td>+60°C</td>
</tr>
<tr>
<td>RH</td>
<td>10%</td>
<td>90%</td>
</tr>
<tr>
<td>VDD</td>
<td>0v</td>
<td>+5.25v</td>
</tr>
</tbody>
</table>

Notes:
These are stress ratings only. Extended exposure to the absolute maximum ratings listed above may affect device reliability or cause permanent damage. Functional operation of the display module at these conditions beyond those listed under Recommended DC Characteristics (Pg. 12) is not implied.

Changes in temperature can result in changes in contrast.
## RECOMMENDED DC CHARACTERISTICS

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<th>DC CHARACTERISTICS</th>
<th>TEST CONDITIONS</th>
<th>SYMBOL</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage for Logic</td>
<td>$T_{OP} = 0^\circ C$ to $+50^\circ C$</td>
<td>$V_{DD} - GND$</td>
<td>+4.75\text{V}</td>
<td>+5.0\text{V}</td>
<td>+5.25\text{V}$^1$</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>$V_{DD} = +5\text{V}$</td>
<td>$V_{IH}$</td>
<td>$V_{DD} - 1.0\text{V}$</td>
<td>$V_{DD}$</td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td></td>
<td>$V_{IL}$</td>
<td>0\text{V}(GND)</td>
<td>+0.60\text{V}</td>
<td></td>
</tr>
<tr>
<td>Output High Voltage</td>
<td></td>
<td>$V_{OH}$</td>
<td>+0.1\text{V}_{DD}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td></td>
<td>$V_{OL}$</td>
<td>0\text{V}(GND)</td>
<td>+0.1\text{V}_{DD}</td>
<td></td>
</tr>
</tbody>
</table>

$^1$Do not exceed +5.25\text{V} maximum.
CURRENT CONSUMPTION

Variables that affect current consumption include the choice of color, brightness of backlights, power supply voltage, and whether or not a PCBA (System Cooling Accessory Board) is attached to the display module.

<table>
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<th>PLCD-35 TYPICAL CURRENT CONSUMPTION (VDD = +5.0v)</th>
<th>BACKLIGHT ONLY</th>
<th>INCLUDING LOGIC</th>
</tr>
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<tr>
<td>Logic + USB controller, backlight off</td>
<td>30 mA</td>
<td></td>
</tr>
<tr>
<td>Logic + USB controller, backlight at 100%</td>
<td>60 mA</td>
<td>90 mA</td>
</tr>
</tbody>
</table>

GPIO CURRENT LIMITS

<table>
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<th>TYPICAL GPIO CURRENT LIMITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sink</td>
</tr>
<tr>
<td>Source</td>
</tr>
</tbody>
</table>

ESD (ELECTRO-STATIC DISCHARGE) SPECIFICATIONS

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

BACKLIGHT FAN AND CRITERIA

<table>
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<th>BACKLIGHT AND FAN(^1) CRITERIA</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backlight PWM(^2) Frequency</td>
<td>320 Hz nominal</td>
</tr>
<tr>
<td>Fan Tachometer Speed Range</td>
<td>600 RPM to 3,000,000 RPM</td>
</tr>
<tr>
<td>(assuming two PPR(^3))</td>
<td></td>
</tr>
<tr>
<td>Fan Power Control PWM(^2) Frequency</td>
<td>18 Hz nominal</td>
</tr>
</tbody>
</table>

\(^1\)Optional PCBA is required to add fans.
\(^2\)PWM is Pulse Width Modulation. PWM is a way to simulate intermediate levels by switching a level between full on and full off. PWM can be used to control the brightness of LED backlights, relying on the natural averaging done by the human eye, as well as for controlling fan power.

\(^3\)PPR is Pulses Per Revolution, can also written as p/r.
OPTICAL SPECIFICATIONS

OPTICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>ITEM</th>
<th>SYMBOL</th>
<th>CONDITION</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Condition for all: $T = 25^\circ$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Viewing Angle</td>
<td>Deg $\theta = 0^\circ$</td>
<td>(12 o’clock) CR$\geq 2$</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deg $\theta = 90^\circ$</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deg $\theta = 180^\circ$</td>
<td></td>
<td></td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deg $\theta = 270^\circ$</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contrast Ratio$^1$</td>
<td>CR</td>
<td>$\theta = 0^\circ$</td>
<td>$\geq 5$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCD Response Time$^2,3$</td>
<td>T rise</td>
<td>100 ms</td>
<td>150 ms</td>
<td>200 ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>T fall</td>
<td>100 ms</td>
<td>150 ms</td>
<td>200 ms</td>
<td></td>
</tr>
</tbody>
</table>

$^1$Contrast Ratio = (brightness with pixels light)/(brightness with pixels dark).
$^2$Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again.
$^3$For reference only.

TEST CONDITIONS AND DEFINITIONS FOR OPTICAL CHARACTERISTICS

We work to continuously improve our products, including backlights that are brighter and last longer. Slight color variations from display module to display module and batch to batch are normal.

- Viewing Angle
  - Vertical (V)$\theta$: $0^\circ$
  - Horizontal (H)$\psi$: $0^\circ$
- Frame Frequency: 78 Hz
- Driving Waveform: 1/16 Duty, 1/13 Bias
- Ambient Temperature (Ta): 25°C
Definition Of Optimal Contrast Setting

CR = \frac{L_{on}}{L_{off}}

L_{on} = \text{Luminance of ON segments}
L_{off} = \text{Luminance of OFF segments}

Unselected State

Selected State

Unselected State

Light Transmitted

Light Blocked

Tr = \text{Rise Time}
Tf = \text{Fall Time}

Figure 4. Definition Of Optimal Contrast Setting (Negative Image)

Figure 5. Definition Of Response Time (Tr, Tf) (Negative Image)
Definition Of 6 O'Clock And 12:00 O'Clock Viewing Angles

These modules have a 12:00 o'clock viewing angle.

![Diagram of 6:00 and 12:00 viewing angles](image)

**Figure 6.** Definition of 6:00 O'clock and 12:00 O'clock Viewing Angles

Definition Of Vertical And Horizontal Viewing Angles (CR>2)

![Diagram of vertical and horizontal viewing angles](image)

**Figure 7.** Definition Of Horizontal And Vertical Viewing Angles (CR>2)
LED BACKLIGHT INFORMATION

Note
For PLCD-35 with white backlights, we recommend that the display be dimmed or turned off during periods of inactivity to conserve the LEDs’ lifetime.

CONNECTION INFORMATION

BUY CABLES SEPARATELY
When you order a PLCD-35, we also offer a choice of cables. The table below has descriptions of common connection configurations. Cable lengths are approximate.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Cable Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>All Cables are RoHS Compliant</td>
</tr>
</tbody>
</table>

USB Cables

Note: The PLCD-35 uses a nonstandard 2 mm low profile connector. USB cables with this type of connector are not readily available at retail stores.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY03</td>
<td>~6 ft. 4.35 inches</td>
</tr>
<tr>
<td>CY11</td>
<td>~2 ft. 6 inches</td>
</tr>
<tr>
<td>CY33</td>
<td>~2 ft. 3.15 inches</td>
</tr>
<tr>
<td>CY24</td>
<td>~2 ft. 1.95 inches</td>
</tr>
</tbody>
</table>

- CY03: The cable has two different types of USB connectors, one smaller than the other. Connect the cable’s smaller 2 mm female USB connector to the display module’s 2 mm male USB connector. Connect the cable’s larger USB-A female connector to host’s USB-A connector.
- CY11: Connect the cable’s 2 mm female USB connector to the display module’s USB connector. Connect the four single pin connectors (Ground, +5v, -D, and +D) to the USB pins on your motherboard.
- CY33: Connect the cable’s smaller 2 mm female USB connector to the display module’s 2 mm male USB connector. Connect the cable’s larger female 4-pin 0.1” connector to the USB pins on your host’s motherboard. For correct orientation, note the +5v location on the 4-pin connector.
- CY24: Add this cable for powering the display module separately from USB. Connect the cable’s 16-pin female connector to the display module’s 16-pin male H1 connector. Connect the cable’s 4-pin male connector to host’s power supply. Note: Open JP2 to avoid back-powering USB.

Cables for ATX Functionality (Power Off, Power On, & Reset) Without Optional PCBA

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY25</td>
<td>~11 inches</td>
</tr>
</tbody>
</table>

Use this ATX power cable to turn an ATX power supply on and off, or power cycle the host through the PLCD-35. Connect the cable’s 16-pin female connector to the PLCD-35’s 16-pin male H1 connector. Connect the cable’s 4-pin ATX connector to the host’s ATX power supply. And connect the cable’s 4 separate female pins to the appropriate 4 pins on the host’s motherboard. (Cable pins are labeled.)

Cables For Optional PCBA

Note: The PLCD-35 does not supply power to the PCBA. The PCBA requires external power, typically supplied by a 4-pin 3.5-inch floppy drive power connector.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY12</td>
<td>~1 ft. 0.55 inches</td>
</tr>
</tbody>
</table>

4-pin hard drive to floppy connector and splitter power cable. Connect the cable’s 4-pin female connector to the PCBA’s male J3 connector. Connect the cable’s male 4-pin floppy power connector to the host’s power supply. Connect the cable’s Reset and Power wires, and the WOL connector to the host’s motherboard.
USB CONNECTION TO HOST

The PLCD-35 is a USB peripheral, requiring only one connection to the host for both data communications and power supply. The PLCD-35 uses a low profile 2 mm latching polarized connector for USB connection.

We can offer three cables to connect between the PLCD-35 and the host:

- The CY03 (~6 ft. 4.35 inches) The cable has two different types of USB connectors, one smaller than the other. Connect the cable’s smaller 2 mm female USB connector to the PLCD-35’s 2 mm male USB connector. Connect the cable’s larger USB-A female connector to host’s USB-A connector.
- The CY11 (~2 ft. 6 inches) has a mating 2 mm connector on one end and standard single pin connectors on the opposite end. These single pin connectors are suitable to plug directly onto the USB headers typically found on motherboards.
- The CY33 (~2 ft. 3.15 inches) Connect the cable’s smaller 2 mm female USB connector to the PLCD-35’s 2 mm male USB connector. Connect the cable’s larger female 4-pin 0.1”connector to the USB pins on your host’s motherboard.

If you would like to make your own cable, the USB connector on the PLCD-35 is:
- FCI/Berg 95000-004LF: SMT 2 mm connector, 4-position, polarized

The mating housing and crimping contact for the cable are:
- FCI/Berg 90312-004: Housing, 2 mm connector, 4-position, polarized
- FCI/Berg 77138-001: Crimping Contact (4 pieces required)
Several versions of Microsoft signed drivers and MacIntosh drivers can be requested. If you do Windows updates on your PC, Windows USB drivers are automatically included.

**H1 CONNECTOR PIN ASSIGNMENTS - INCLUDES FIVE GPIOS**

PLCD-35 has five GPIOs available on connector H1. These GPIOs can be accessed directly through H1 or through the optional PCBA (System Cooling Accessory Board) when it is connected to H1.

*Note: F1P through F4P and F1T through F4T are reserved for fans with optional SCAB.*

![H1 Connector Diagram]

Please see the commands 34 (0x22): GPIO Settings (PCBA Required) (Pg. 48), and 35 (0x23): Read GPIO Pin Levels And Configuration State (PCBA Required) (Pg. 50) below for details on how to control the GPIOs.

The following parts may be used to make a mating cable for H1:
- 16-position housing: Hirose DF11-16DS-2C / Digi-Key H2025-ND.
- Crimping contact (tape & reel): Hirose DF11-2428SCF / Digi-Key H1504TR-ND.
- Crimping contact (loose): Hirose DF11-2428SC / Digi-Key H1504-ND.
- Pre-terminated interconnect wire: Hirose / Digi-Key H3BBT-10112-B4-ND is typical.

For descriptions of cables that connect to H1, see table descriptions in Buy Cables Separately (Pg. 17).
**ATX POWER SUPPLY**

**ATX Power And Control Connections**

- ATX power supply control functionality allows the buttons on the PLCD-35 to replace the power and reset button on your system, simplifying front panel design. This ATX power supply control functionality can be accomplished with the optional PCBA+CY14 ATX power cable or use the CY25 or CY38 ATX power cable without the PCBA. The PCBA provides fan monitoring and control as well as DOW temperature sensor monitoring.

When configuring the PLCD-35 for ATX functionality, open jumper JP2 in order to ensure correct operation. See **ELECTRICAL SPECIFICATIONS (Pg. 10)**. This is required whether the optional PCBA is or is not used.

ATX configuration for the PLCD-35 is powered from the PC's VSB signal, the “stand-by” or “always-on” +5v ATX power supply output, on pins 15 and 16 of the H1 connector. When using the optional PCBA, the +5 standby voltage is supplied on the 7-pin header pins labeled GND and +5v.

**GPIO[1] ATX Host Power Sense**
Since the PLCD-35 must act differently depending on whether the host's power supply is on or off, you must also connect the host's “switched +5v” to GPIO[1]. This GPIO line functions as POWER SENSE. The POWER SENSE pin is configured as an input with a pull-down, 5kΩ nominal.

**GPIO[2] ATX Host Power Control**
The motherboard's power switch input is connected to GPIO[2]. This GPIO line functions as POWER CONTROL. The POWER CONTROL pin is configured as a high impedance input until the display module instructs the host to turn on or off. Then it will change momentarily to low impedance output, driving either low or high depending on the setting of POWER INVERT. See command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44).

**GPIO[3] ATX Host Reset Control**
The motherboard's reset switch input is connected to GPIO[3]. This GPIO line functions as RESET. The RESET pin is configured as a high-impedance input until the display module wants to RESET the host. Then it will change momentarily to low impedance output, driving either low or high depending on the setting of RESET_INVERT. See command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44). This connection is also used for the hardware watchdog.

---

### Table: ATX Power Supply & Control Connections

<table>
<thead>
<tr>
<th>ATX Power Supply &amp; Control Connections</th>
<th>With Optional PCBA*</th>
<th>Without Optional PCBA Pins on Connector H1</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{SB}, +5v</td>
<td>PCBA’s 7-pin header, +5v</td>
<td>Pin 16</td>
</tr>
<tr>
<td>V_{SB}, Ground</td>
<td>PCBA’s 7-pin header, GND</td>
<td>Pin 15</td>
</tr>
<tr>
<td>GPIO[1] ATX Host Power Sense</td>
<td>PCBA’s 4-pin power header, +5v</td>
<td>Pin 12</td>
</tr>
</tbody>
</table>

*PCBA’s JP8 must be open and JP9 must be closed. For details, see the PCBA Data Sheet.*
ATX Connection With Optional PCBA Using CY14 Cable

The CY14 cable allows ATX power control connections through the optional PCBA. This allows additional flexibility in cabling and overall functionality of the PLCD-35 in system control and monitoring. Buy the CY15 or CY19 to connect the PCBA to the PLCD-35's connector H1.

Note
If the CY14 cable and PCBA are ordered at the same time as the PLCD-35 through we will open JP2 on the PLCD-35, open JP8 and close JP9 on the PCBA, and send the following software configuration commands.

Once these changes are made, for the PLCD-35 to power up, power must be applied to the 7-pin header on the PCBA as well as the 4-pin power header. If you do not want these jumper changes when you order a PLCD-35 and PCBA, please write a note in the Special Instructions box.

```plaintext
command = 28  // Set ATX Switch Functionality
length = 1
data[0] = 240 // Enable:
   //   KEYPAD_POWER_OFF
   //   KEYPAD_POWER_ON
   //   KEYPAD_RESET
   //   LCD_OFF_IF_HOST_IS_OFF
command = 4   // Store current state as boot state
length = 0
```
The illustration below shows how:

- Optional PCBA connects to the display module using a CY19 cable (or CY15 can be used).
- How the optional PCBA connects to your host's motherboard using a CY14 cable.

Note: For ATX functionality,
- JP8 must be open.
- JP9 must be closed.

Figure 9. ATX Connection With Optional PCBA Using CY14 ATX Cable
ATX Connection Without PCBA Using CY25 ATX Cable

The optional CY25 cable simplifies ATX power control connections, allowing all ATX power supply control functionality through the PLCD-35’s H1 connector.

**Note**
If the CY25 cable is ordered at the same time as the display module, we will open jumper JP2 and send the following software configuration commands unless we are otherwise instructed. Please note that once these changes are made, for the display module to power up, power must be applied to connector H1 with +5v applied to pin 15 and ground to pin 16.

```plaintext
command = 28  // Set ATX Switch Functionality
length = 1
data[0] = 240 // Enable:
    //   KEYPAD_POWER_OFF
    //   KEYPAD_POWER_ON
    //   KEYPAD_RESET
    //   LCD_OFF_IF_HOST_IS_OFF
command = 4   // Store current state as boot state
length = 0
```

Below is an illustration of how the optional CY25 cable connects to the PLCD-35’s H1 connector and your system’s motherboard and ATX power supply:

![Figure 10. ATX Power Supply And Control Connections Using CY25 ATX Cable](image-url)
HOW TO SET ATX FUNCTIONALITY USING THE APPLICATION

1. Request the appropriate application.
2. Connect the PLCD-35 to a Windows' based PC. You may want to connect the +5VSB and +5VSENSE so you will be able to see the PLCD-35 when it powers up.
3. Disable any applications that communicate with the PLCD-35 to free up the virtual COM port.
4. Launch the application. The application should automatically recognize the PLCD-35 and display it in the Communications Port dropdown list. If not, select your PLCD-35 from the dropdown list.
5. In the Send Packet section, select command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44) from the dropdown list.
6. Type in the following value: "\240" into the Data field. The "\240" represents the bitmask value for data[0].
7. Click Send Packet.
8. Select command 4 (0x04): Store Current State As Boot State (Pg. 29) from The PacketType dropdown list.
9. Clear the Data text box.
10. Click Send Packet. This saves the current state set with ATX.

HOW TO CONNECT THE OPTIONAL PCBA

The optional PCBA is designed to connect to a PLCD-35's H1 connector. The PCBA will receive the correct signals to operate from the display module.

Two cables are available to make the connection between the PCBA and the PLCD-35:

1. CY15 PCBA cable (~16-inch)
   This cable allows the PCBA to be mounted some distance away from the PLCD-35. For instance, the PCBA could be mounted in a central location within a PC's case. The CY15 would connect from this central location to the display module that is mounted in a drive bay. Then the connections to the fans and temperature sensors only need to be run to the PCBA, not all the way to the front panel where the PLCD-35 is mounted.

2. CY19 cable (~3.5-inch)
   This cable can used when the PCBA is mounted close to the PLCD-35, as is the case when the PCBA is fastened directly to the PLCD-35's built-in drive bay bracket.

HOST COMMUNICATIONS

Note:
Where “PLCD-35 with ATX” is described, you can use any of these: CY25 ATX power cable, CY38 power cable, or PCBA+CY14 ATX power cable

PLCD-35 communicates with its host using the USB interface. The easiest and most common way for the host software to access the USB is through the virtual COM port (VCP) drivers. Several versions of Microsoft signed drivers and MacIntosh drivers can be downloaded. Please ask if you need this. If you do Windows updates on your PC, Windows USB drivers are automatically included. Using these drivers makes it appear to the host software as if there is an additional serial port (the VCP) on the host system when the PLCD-35 is connected. This VCP should be opened at 115200 baud, 8 data bits, no parity, 1 stop bit.
 PACKET STRUCTURE

All communication between the PLCD-35 and the host takes place in the form of a simple and robust CRC checked packet. The packet format allows for very reliable communications between the PLCD-35 and the host without the traditional problems that occur in a stream-based serial communication (such as having to send data in inefficient ASCII format, to “escape” certain “control characters”, or losing sync if a character is corrupted, missing, or inserted).

All packets have the following structure:

\[ \text{<type><data_length><data><CRC>} \]

type is one byte, and identifies the type and function of the packet:

\[ TTcc \text{ cccc} \]

\[ ||| \text{ ||||}--\text{Command, response, error or report code 0-63} \]

\[ --------Type: \]

\[ 00 = \text{normal command from host to PLCD-35} \]

\[ 01 = \text{normal response from PLCD-35 to host} \]

\[ 10 = \text{normal report from PLCD-35 to host (not in direct response to a command from the host)} \]

\[ 11 = \text{error response from PLCD-35 to host (a packet with valid structure but illegal content was received by the PLCD-35)} \]

data_length specifies the number of bytes that will follow in the data field. The valid range of \text{data_length} is 0 to 22.

data is the payload of the packet. Each type of packet will have a specified \text{data_length} and format for \text{data} as well as algorithms for decoding \text{data} detailed below.

\text{CRC} is a standard 16-bit CRC of all the bytes in the packet except the CRC itself. The CRC is sent LSB first. At the port, the CRC immediately follows the last used element of data \{1\}. See Sample Algorithms To Calculate The CRC (Pg. 66) for details.

The following C definition may be useful for understanding the packet structure.

```c
typedef struct
{
    unsigned char
        command;
    unsigned char
        data_length;
    unsigned char
        data[MAX_DATA_LENGTH];
    unsigned short
        CRC;
} COMMAND_PACKET;
```

We can supply a demonstration and test program for Windows. The application allows you to experiment with the command set described below.

Note

Reconciling packets is recommended rather than using delays when communicating with the display module. To reconcile your packets, please ensure that you have received the acknowledgment packet from the packet most recently sent before sending any additional packets to the display module. This practice will guarantee that you will not have any dropped packets or missed communication with the display module.
ABOUT HANDSHAKING

The nature of PLCD-35’s packets makes it unnecessary to implement traditional hardware or software handshaking.

The host should wait for a corresponding acknowledge packet from the PLCD-35 before sending the next command packet. The PLCD-35 will respond to all packets within 250 mS. The host software should stop waiting and retry the packet if the PLCD-35 fails to respond within 250 mS. The host software should report an error if a packet is not acknowledged after several retries. This situation indicates a hardware problem — for example, a disconnected cable.

Please note that some operating systems may introduce delays between when the data arrives at the physical port from the PLCD-35 until it is available to the user program. In this case, the host program may have to increase its timeout window to account for the additional overhead of the operating system.

The PLCD-35 can be configured to send several types of report packets along with regular acknowledge packets. The host should be able to buffer several incoming packets and must guarantee that it can process and remove packets from its input buffer faster than the packets can arrive given the 115200 baud rate of the VCP and the reporting configuration of the PLCD-35. For any modern PC using reasonably efficient software, this requirement will not be a challenge.

The report packets are sent asynchronously with respect to the command packets received from the host. The host should not assume that the first packet received after it sends a command is the acknowledge packet for that command. The host should inspect the type field of incoming packets and process them accordingly.

REPORT CODES

The PLCD-35 can be configured to report three items. The PLCD-35 sends reports automatically when the data becomes available. Reports are not sent in response to a particular packet received from the host. The three report types are (1) 0x80: Key Activity, (2) 0x81: Fan Speed Report (PCBA Required), and (3) 0x82: Temperature Sensor Report (PCBA Required). Details are below.

0x80: Key Activity

If a key is pressed or released, the PLCD-35 sends a Key Activity report packet to the host. Key event reporting may be individually enabled or disabled by command 23 (0x17): Configure Key Reporting (Pg. 41).

```plaintext
type = 0x80
data_length = 1
data[0] is the type of keyboard activity:
KEY_UL_PRESS 13
KEY_UR_PRESS 14
KEY_LL_PRESS 15
KEY_LR_PRESS 16
KEY_UL_RELEASE 17
KEY_UR_RELEASE 18
KEY_LL_RELEASE 19
KEY_LR_RELEASE 20
```

0x81: Fan Speed Report (PCBA Required)

If any of up to four fans connected to PLCD-35+PCBA is configured to report its speed information to the host, the PLCD-35 will send Fan Speed Reports for each selected fan every 1/2 second. See command 16 (0x10): Set Up Fan Reporting (PCBA Required) (Pg. 36).
type = 0x81
data_length = 4
data[0] is the index of the fan being reported:
0 = FAN 1
1 = FAN 2
2 = FAN 3
3 = FAN 4
data[1] is number_of_fan_tach_cycles
data[2] is the MSB of Fan_Timer_Ticks
data[3] is the LSB of Fan_Timer_Ticks

The following C function will decode the fan speed from a Fan Speed Report packet into RPM:

```c
int OnReceivedFanReport(COMMAND_PACKET *packet, char * output)
{
    int
    return_value=0;

    int
    number_of_fan_tach_cycles;
    number_of_fan_tach_cycles=packet->data[1];

    if(number_of_fan_tach_cycles<3)
        sprintf(output," STOP");
    else if(number_of_fan_tach_cycles<4)
        sprintf(output," SLOW");
    else if(0xFF==number_of_fan_tach_cycles)
        sprintf(output," ----");
    else
    {
        //Specific to each fan, most commonly 2
        int
        pulses_per_revolution;
        pulses_per_revolution=2;

        int
        Fan_Timer_Ticks;
        Fan_Timer_Ticks=(*(unsigned short *)&(packet->data[2]));

        return_value=((27692308L/pulses_per_revolution)*
                      (unsigned long)(number_of_fan_tach_cycles-3))/
                      (Fan_Timer_Ticks);
        sprintf(output,%5d,return_value);
    }
    return(return_value);
}
```

0x82: Temperature Sensor Report (PCBA Required)

If any of the up to 32 temperature sensors is configured to report to the host, the PLCD-35+PCBA will send Temperature Sensor Reports for each selected sensor every second. See the command 19 (0x13): Set Up CY17 Temperature Reporting (PCBA Required) (Pg. 37).

type = 0x82
data_length = 4
data[0] is the index of the temperature sensor being reported:
0 = temperature sensor 1
1 = temperature sensor 2
...
31 = temperature sensor 32
data[1] is the MSB of Temperature_Sensor_Counts
data[2] is the LSB of Temperature_Sensor_Counts
data[3] is DOW_crc_status
The following C function will decode the Temperature Sensor Report packet into °C and °F:

```c
void OnReceivedTempReport(COMMAND_PACKET *packet, char *output)
{
    // First check the DOW CRC return code from the PLCD-35
    if(packet->data[3]==0)
        strcpy(output,"BAD CRC");
    else
    {
        double
degc;
        degc=(*(short *)&(packet->data[1]))/16.0;
        double
degf;
        degf=(degc*9.0)/5.0+32.0;
        sprintf(output,"%9.4f°C =%9.4f°F",
                degc,
                degf);
    }
}
```

### COMMAND CODES

Below is a list of valid commands for the PLCD-35. The commands are in numerical order, with command 15 intentionally left out.

Each command packet is answered by either a response packet or an error packet. The low 6 bits of the type field of the response or error packet is the same as the low 6 bits of the type field of the command packet being acknowledged.

**0 (0x00): Ping Command**

Used to verify communication with the PLCD-35. The PLCD-35 will echo the Ping Command to the host.

- **type:** 0x00 = 010
- **valid data_length is 0 to 16**
- **data[0-(data_length-1)] can be filled with any arbitrary data**

The return packet is identical to the packet sent, except the type will be 0x40 (normal response, Ping Command):

- **type:** 0x40 | 0x00 = 0x40 = 6410
- **data_length = (identical to received packet)**
- **data[0-(data_length-1)] = (identical to received packet)**

**1 (0x01): Get Hardware And Firmware Version**

The PLCD-35 will return the hardware and firmware version information to the host.

- **type:** 0x01 = 110
- **valid data_length is 0**

The return packet will be:

- **type:** 0x40 | 0x01 = 0x41 = 6510
- **data_length = 16**
- **data[] = "PLCD-35:XhX,uYvY"**

XhX is the hardware revision.
uYvY is the firmware version.

**2 (0x02): Write User Flash Area**

The PLCD-35 reserves 16 bytes of nonvolatile memory for arbitrary use by the host. This memory can be used to store a serial number, IP address, gateway address, netmask, or any other data required. All 16 bytes must be supplied.
type: 0x02 = 210
valid data_length is 16
data[] = 16 bytes of arbitrary user data to be stored in the PLCD-35's nonvolatile memory

The return packet will be:
  type: 0x40 | 0x02 = 0x42 = 6610
  data_length = 0

3 (0x03): Read User Flash Area

This command will read the User Flash Area and return the data to the host.
  type: 0x03 = 310
  valid data_length is 0

The return packet will be:
  type: 0x40 | 0x03 = 0x43 = 6710
  data_length = 16
  data[] = 16 bytes user data recalled from the PLCD-35's nonvolatile memory

4 (0x04): Store Current State As Boot State

The PLCD-35 loads its power-up configuration from nonvolatile memory when power is applied. The PLCD-35 is configured at the factory to display a "welcome" bootscreen when power is applied. This command can be used to customize the "welcome" screen, as well as the following items:

- Characters shown on display, which are affected by:
  - Command 6 (0x06): Clear Display (Pg. 33).
  - Command 7 (0x07): Set Display Contents, Line 1 (CFA633 Compatible) (Pg. 33).
  - Command 8 (0x08): Set Display Contents, Line 2 (CFA633 Compatible) (Pg. 33).
  - Command 31 (0x1F): Send Data To Display (Pg. 47).
- Special character font definitions (command 9 (0x09): Set Display Special Character Data (Pg. 34)).
- Cursor position (command 11 (0x0B): Set Display Cursor Position (Pg. 34)).
- Cursor style (command 12 (0x0C): Set Display Cursor Style (Pg. 35)).
- Contrast setting (command 13 (0x0D): Set Display Contrast (Pg. 35)).
- Backlight setting (command 14 (0x0E): Set Display And Keypad Backlights (Pg. 35)).
- Fan power settings (command 17 (0x11): Set Fan Power (PCBA Required) (Pg. 36)).
- Settings of any "live" displays (command 21 (0x15): Set Up Live Fan Or Temperature Display (PCBA Required) (Pg. 39)).
- Key press and release masks (command 23 (0x17): Configure Key Reporting (Pg. 41)).
- Fan glitch delay settings (command 26 (0x1A): Set Fan Tachometer Glitch Delay (PCBA Required) (Pg. 42)).
- ATX function enable and pulse length settings (command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44)).
- Key legends (command 32: Key Legends (Pg. 47)).
- Baud rate (command 33 (0x21): Set Baud Rate (Pg. 48)).
- GPIO settings (command 34 (0x22): GPIO Settings (PCBA Required) (Pg. 48)).

You cannot store the fan or temperature reporting, although the live display of fans or temperatures can be saved. You cannot store the fan fail-safe or host watchdog. The host software should enable these items once the system is initialized and it is ready to receive the data.

  type: 0x04 = 410
  valid data_length is 0
The return packet will be:

\[
\begin{align*}
\text{type: } & \, 0x40 \mid 0x04 = 0x44 = 68_{10} \\
\text{data\_length} & = 0
\end{align*}
\]

If the current state and the boot state do not match after saving, the display module will return an error instead of an ACK. In this unlikely error case, the boot state will be undefined.

5 (0x05): Reboot PLCD-35, Reset Host, or Power Off Host Using ATX

For ATX CY25 and CY38 ATX power cables or the optional PCBA+CY14 ATX power cable is required.

This command instructs the PLCD-35 with ATX to simulate a power-on restart of itself, reset the host, or turn the host's power off. The ability to reset the host may be useful to allow certain host operating system configuration changes to complete. The ability to turn the host's power off under software control may be useful in systems that do not have ACPI* compatible BIOS.

*Advanced Configuration and Power Interface) is an industry specification for the efficient handling of power consumption in desktop and mobile computers.

Note

The GPIO pins used for ATX control must not be configured as user GPIO. The GPIO pins must be configured to their default drive mode in order for the ATX functions to work correctly. These settings are factory default but may be changed by the user. Please see command 34 (0x22): GPIO Settings (PCBA Required).

Rebooting the PLCD-35 may be useful when testing the boot configuration. It may also be useful to re-enumerate the optional CY17 temperature sensors on the 1-Wire bus (optional PCBA required).

To reboot the PLCD-35, send the following packet:

\[
\begin{align*}
\text{type} & = 0x05 = 5_{10} \\
\text{valid data\_length is} & = 3 \\
\text{data[0]} & = 8 \\
\text{data[1]} & = 18 \\
\text{data[2]} & = 99
\end{align*}
\]
To reset the host using PLCD-35 with ATX, assuming the host's reset line is connected to GPIO[3] as described in command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44), send the following packet:

\[
\begin{align*}
type &= 0x05 = 5_{10} \\
valid\ data\ length\ &= 3 \\
data[0] &= 12 \\
data[1] &= 28 \\
data[2] &= 97
\end{align*}
\]

To turn the host's power off using PLCD-35 with ATX, assuming the host's power control line is connected to GPIO[2] as described in command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44), send the following packet:

\[
\begin{align*}
type &= 0x05 = 5_{10} \\
valid\ data\ length\ &= 3 \\
data[0] &= 3 \\
data[1] &= 11 \\
data[2] &= 95
\end{align*}
\]

Note

The PLCD-35 will return the acknowledge packet immediately, then reset the host. After resetting the host (~1.5 seconds), the display module will reboot itself. The display module will not respond to new command packets for up to 3 seconds (~4.5 seconds overall) after its reboot. Part of this delay is the intentional staggered sequencing of turning on power to the fans. If you are not using fans, you can speed the boot process by setting the fan power to 0 (command 17 (0x11): Set Fan Power (PCBA Required) and saving this as the default boot state (command 4 (0x04): Store Current State As Boot State). Normally, the host will be recovering from its own reset, so the boot delay of the display module will not be of consequence.

Note On Bootup Delay If Using Fans (Optional PCBA Required)

The reboot command may take up to 3 seconds to return its acknowledge packet.

At bootup, there is up to a 500ms (1/2 second) delay between turning on fans. By default, all fans are set to "on" at 100%. If you are not using a fan, set power to 0% (command 17 (0x11): Set Fan Power (PCBA Required) (Pg. 36) and save this setting as the default boot state (command 4 (0x04): Store Current State As Boot State (Pg. 29)). This will reduce the boot time.

<table>
<thead>
<tr>
<th># of Fans Powered On</th>
<th>Expected Boot Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to 1</td>
<td>300ms - 500ms</td>
</tr>
<tr>
<td>2</td>
<td>800ms - 1,000ms</td>
</tr>
<tr>
<td>3</td>
<td>1.3s - 1.5s</td>
</tr>
<tr>
<td>4</td>
<td>1.8s - 2.0s</td>
</tr>
</tbody>
</table>

To turn the host's power off using PLCD-35 with ATX, assuming the host's power control line is connected to GPIO[2] as described in command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44), send the following packet:

\[
\begin{align*}
type &= 0x05 = 5_{10} \\
valid\ data\ length\ &= 3 \\
data[0] &= 3 \\
data[1] &= 11 \\
data[2] &= 95
\end{align*}
\]
In any of the above cases, the return packet will be:

\[
\text{type} = 0x40 \mid 0x05 = 0x45 = 69_{10}
\]
\[
data\_length = 0
\]

To reset the host, assuming the host's reset line is connected to GPIO[3] as described in command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44), send the following packet:

\[
\text{type}: 0x05 = 5_{10}
\]
\[
\text{valid data length is 3}
\]
\[
data[0] = 12
\]
\[
data[1] = 28
\]
\[
data[2] = 97
\]

Note
The PLCD-35 will return the acknowledge packet immediately, then reset the host. After resetting the host (~1.5 seconds), the display module will reboot itself. The display module will not respond to new command packets for up to 3 seconds (~4.5 seconds overall) after its reboot. Part of this delay is the intentional staggered sequencing of turning on power to the fans. If you are not using fans, you can speed the boot process by setting the fan power to 0 (command 17 (0x11): Set Fan Power (PCBA Required) and saving this as the default boot state (command 4 (0x04): Store Current State As Boot State). Normally, the host will be recovering from its own reset, so the boot delay of the display module will not be of consequence.

To turn the host's power off, assuming the host's power control line is connected to GPIO[2] as described in command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44), send the following packet:

\[
\text{type}: 0x05 = 5_{10}
\]
\[
\text{valid data length is 3}
\]
\[
data[0] = 3
\]
\[
data[1] = 11
\]
\[
data[2] = 95
\]

Note
The PLCD-35 will return the acknowledge packet immediately, then power cycle the host. The power cycle length is dependent on the length of the power pulse (command 28 (0x1C): Set ATX Power Switch Functionality). After power cycling the host, the display module will reboot itself. The display module will not respond to new command packets for up to 3 seconds after its reboot. Part of this delay is the intentional staggered sequencing of turning on power to the fans. If you are not using fans, you can speed the boot process by setting the fan power to 0 (command 17 (0x11): Set Fan Power (PCBA Required) and saving this as the default boot state (command 4 (0x04): Store Current State As Boot State). Normally the host will be off or recovering from its own power cycle, so the boot delay of the display module will not be of consequence.

In any of the above cases, the return packet will be:

\[
\text{type}: 0x40 \mid 0x05 = 0x45 = 69_{10}
\]
\[
data\_length = 0
\]
6 (0x06): Clear Display
Sets the contents of the display screen DDRAM to ‘ ‘ = 0x20 = 32 and moves the cursor to the left-most column of the top line.

\[
\begin{align*}
\text{type: } & \ 0x06 = 6_{10} \\
\text{valid data_length is } & \ 0
\end{align*}
\]

The return packet will be:

\[
\begin{align*}
\text{type: } & \ 0x40 \ | \ 0x06 = 0x46 = 70_{10} \\
\text{data_length} = & \ 0
\end{align*}
\]

Clear Display changes the display screen. The display contents is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

7 (0x07): Set Display Contents, Line 1 (CFA633 Compatible)
Sets the center 16 characters displayed for the top line of the display. The first two and last two characters are blanked.

\[
\begin{align*}
\text{type: } & \ 0x7 = 7_{10} \\
\text{valid data_length is } & \ 16 \\
\text{data[]} = & \ \text{top line’s display content (must supply 16 bytes)}
\end{align*}
\]

The return packet will be:

\[
\begin{align*}
\text{type: } & \ 0x40 \ | \ 0x07 = 0x47 = 71_{10} \\
\text{data_length} = & \ 0
\end{align*}
\]

Set Display Contents, Line 1 is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

8 (0x08): Set Display Contents, Line 2 (CFA633 Compatible)
Sets the center 16 characters displayed for the top line of display. The first two and last two characters are blanked.

\[
\begin{align*}
\text{type: } & \ 0x8 = 8_{10} \\
\text{valid data_length is } & \ 16 \\
\text{data[]} = & \ \text{bottom line's display content (must supply 16 bytes)}
\end{align*}
\]

The return packet will be:

\[
\begin{align*}
\text{type: } & \ 0x40 \ | \ 0x08 = 0x48 = 72_{10} \\
\text{data_length} = & \ 0
\end{align*}
\]

Note
This command allows legacy software that displays data on older CFA633 display modules to work unchanged on the PLCD-35. For new applications, please use the more flexible command 31 (0x1F): Send Data To Display.
Set Display Contents, Line 2 is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

9 (0x09): Set Display Special Character Data

Sets the font definition for one of the special characters (CGROM). (See CHARACTER GENERATOR ROM (CGROM) (Pg. 52))

- type: 0x09 = 9\textsubscript{10}
- valid data length is 9
- data[0] = index of special character that you would like to modify, 0-7 are valid
- data[1-8] = bitmap of the new font for this character

Data[1-8] are the bitmap information for this character. Any value is valid between 0 and 63, the msb is at the left of the character cell of the row, and the lsb is at the right of the character cell. Additionally, if you set bit 7 of any of the data bytes, the entire line of pixels within this character will blink.

- data[1] is at the top of the cell.
- data[8] is at the bottom of the cell.

The return packet will be:

- type: 0x40 | 0x09 = 0x49 = 73\textsubscript{10}
- data_length = 0

Set Display Special Character Data is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

10 (0x0A): Read 8 Bytes of Display Memory

This command will return the contents of the display’s DDRAM or CGROM. This command is intended for debugging.

- type: 0x0A = 10\textsubscript{10}
- valid data length is 1
- data[0] = address code of desired data

Data[0] is the address code native to the display controller:

- 0x40 (\textsubscript{164}) to 0x7F (\textsubscript{127}) for CGROM
- 0x80 (\textsubscript{128}) to 0x93 (\textsubscript{147}) for DDRAM, line 1
- 0xC0 (\textsubscript{192}) to 0xD3 (\textsubscript{211}) for DDRAM, line 2

The return packet will be:

- type: 0x40 | 0x0A = 0x4A = 74\textsubscript{10}
- data_length = 9

Data[0] of the return packet will be the address code.
Data[1-8] of the return packet will be the data read from the display’s controller’s memory.

11 (0x0B): Set Display Cursor Position

This command allows the cursor to be placed at the desired location on the PLCD-35’s display. If you want the cursor to be visible, you may also need to send a command 12 (0x0C): Set Display Cursor Style (Pg. 35).

- type: 0x0B = 11\textsubscript{10}
- valid data length is 2
- data[0] = column (0-19 valid)
- data[1] = row (0-1 valid)

The return packet will be:

- type: 0x40 | 0x0B = 0x4B = 75\textsubscript{10}
- data_length = 0
Set Display Cursor Position is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

12 (0x0C): Set Display Cursor Style

This command allows you to select among four hardware generated cursor options.

- type: 0x0C = 1210
  - valid data_length is 1
  - data[0] = cursor style (0-4 valid)
  - 0 = no cursor.
  - 1 = blinking block cursor.
  - 2 = static underscore cursor.
  - 3 = blinking block plus underscore.
  - 4 = blinking underscore (Behavior is different from previous PLCD-35 versions (firmware v2.0 and earlier.)

The return packet will be:

- type: 0x40 | 0x0C = 0x4C = 7610
- data_length = 0

Set Display Cursor Style is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

13 (0x0D): Set Display Contrast

This command sets the contrast or vertical viewing angle of the display.

- type: 0x0D = 1310
  - valid data_length is 1
  - data[0] = contrast setting (0-254 valid)
  - 60 = light
  - 105 = about right
  - 129 = dark
  - 130-254 = very dark (may be useful at cold temperatures)

The return packet will be:

- type = 0x40 | 0x0D = 0x4D = 7710
- data_length = 0

Set Display Contrast is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

14 (0x0E): Set Display And Keypad Backlights

This command sets the brightness of the display and keypad backlights.

- type: 0x0E = 1410
  - valid data_length is 1
  - data[0] = backlights power setting (0-100 valid)
  - 0 = off
  - 1-99 = variable brightness
  - 100 = on

The return packet will be:

- type: 0x40 | 0x0E = 0x4E = 7810
- data_length = 0

Set Display & Keypad Backlight is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).
16 (0x10): Set Up Fan Reporting (PCBA Required)

This command will configure the PLCD-35+PCBA to report the fan speed information to the host every 500 mS.

\[
\text{type} = 0x10 = 16_{10} \\
\text{valid data length is 1} \\
\text{data}[0] = \text{bitmask indicating which fans are enabled to report (0-15 valid)} \\
\text{---- 8421 Enable Reporting of this Fan’s Tach Input} \\
\text{||| |} -- \text{Fan 1: 1 = enable, 0 = disable} \\
\text{||| ||} -- \text{Fan 2: 1 = enable, 0 = disable} \\
\text{||| |||} -- \text{Fan 3: 1 = enable, 0 = disable} \\
\text{||| ||| |} -- \text{Fan 4: 1 = enable, 0 = disable}
\]

The return packet will be:

\[
\text{type} = 0x40 \mid 0x10 = 0x50 = 80_{10} \\
\text{data_length} = 0
\]

If \text{data}[0] is not 0, then the PLCD-35 will start sending 0x81: Fan Speed Report packets for each enabled fan every 500 mS. (See \text{0x81: Fan Speed Report (PCBA Required)} (Pg. 26).) Each of the report packets is staggered by 1/8 of a second.

Reporting a fan will override the fan power setting to 100% for up to 1/8 of a second every 1/2 second. Please see “Fan Connections” in the PCBA Datasheet for a detailed description.

17 (0x11): Set Fan Power (PCBA Required)

This command will configure the power settings for the fan connectors on the PCBA.

\[
\text{type} = 0x111 = 17_{10} \\
\text{valid data length is 4} \\
\text{data}[0] = \text{power level for FAN 1 (0-100 valid)} \\
\text{data}[1] = \text{power level for FAN 2 (0-100 valid)} \\
\text{data}[2] = \text{power level for FAN 3 (0-100 valid)} \\
\text{data}[3] = \text{power level for FAN 4 (0-100 valid)}
\]

The return packet will be:

\[
\text{type} = 0x40 \mid 0x111 = 0x51 = 81_{10} \\
\text{data_length} = 0
\]

Set Fan Power is one of the items stored by the command \text{4 (0x04): Store Current State As Boot State} (Pg. 29).
18 (0x12): Read CY17 Temperature Sensors (PCBA Required)

When power is applied to the PLCD-35+PCBA+CY17 temperature sensors, it detects any devices (CY17) connected to the DOW bus and stores the device’s information. This command will allow the host to read the device’s information.

**Note**
The GPIO pin used for DOW must not be configured as user GPIO. It must be configured to its default drive mode in order for the DOW functions to work correctly.

These settings are factory default but may be changed by the user. Please see command 34 (0x22): GPIO Settings (PCBA Required) (Pg. 48).

In order for the DOW subsystem to be enabled and operate correctly, user GPIO[4] must be configured as:

\[\text{DDD} = "111: 1=Hi-Z, 0=Slow, Strong Drive Down".\]
\[\text{F} = "0: Port unused for user GPIO."\]

This state is the factory default, but it can be changed and saved by the user. To ensure that GPIO[4] is set correctly and the DOW operation is enabled, send the following command:

```plaintext
command = 34
length = 3
data[0] = 4
data[1] = 100
data[2] = 7
```

This setting must be saved as the boot state, so when the PLCD-35+PCBA reboots, it will detect the CY17 temperature sensors.

- type = 0x12 = 18_{10}
- valid data_length is 1
- data[0] = device index (0-31 valid)

The return packet will be:

```plaintext
type = 0x40 | 0x12 = 0x52 = 82_{10}
data_length = 9
data[0] = device index (0-31 valid)
data[1-8] = ROM ID of the device
```

If data[1] is 0x22 (CY17 temperature sensor), then that device can be set up to automatically convert and report the temperature every second. See the command 19 (0x13): Set Up CY17 Temperature Reporting (PCBA Required) (Pg. 37).

19 (0x13): Set Up CY17 Temperature Reporting (PCBA Required)

This command will configure the PLCD-35+PCBA+CY17 to report the temperature information to the host every second.
type: 0x13 = 1910
valid data_length is 4
data[0-3] = 32-bit bitmask indicating which temperature sensors are enabled to report
(0-255 valid in each location)

data[0]
08 07 06 05 04 03 02 01 Enable Reporting of sensor with device index of:
| | | | |-- 0: 1 = enable, 0 = disable
| | | | ----- 1: 1 = enable, 0 = disable
| | | | --------- 2: 1 = enable, 0 = disable
| | | | ------------ 3: 1 = enable, 0 = disable
| | | | ----------------- 4: 1 = enable, 0 = disable
| | | | --------------------- 5: 1 = enable, 0 = disable
| | | -------------------------- 6: 1 = enable, 0 = disable
| | | |-------------------------- 7: 1 = enable, 0 = disable

data[1]
16 15 14 13 12 11 10 09 Enable Reporting of sensor with device index of:
| | | | |-- 8: 1 = enable, 0 = disable
| | | | ----- 9: 1 = enable, 0 = disable
| | | | --------- 10: 1 = enable, 0 = disable
| | | | ------------ 11: 1 = enable, 0 = disable
| | | | ----------------- 12: 1 = enable, 0 = disable
| | | | --------------------- 13: 1 = enable, 0 = disable
| | | |-------------------------- 14: 1 = enable, 0 = disable
| | | -------------------------- 15: 1 = enable, 0 = disable

data[2]
24 23 22 21 20 19 18 17 Enable Reporting of sensor with device index of:
| | | | |-- 16: 1 = enable, 0 = disable
| | | | ----- 17: 1 = enable, 0 = disable
| | | | --------- 18: 1 = enable, 0 = disable
| | | | ------------ 19: 1 = enable, 0 = disable
| | | | ----------------- 20: 1 = enable, 0 = disable
| | | | --------------------- 21: 1 = enable, 0 = disable
| | | |-------------------------- 22: 1 = enable, 0 = disable
| | | -------------------------- 23: 1 = enable, 0 = disable

data[3]
32 31 30 29 28 27 26 25 Enable Reporting of sensor with device index of:
| | | | |-- 24: 1 = enable, 0 = disable
| | | | ----- 25: 1 = enable, 0 = disable
| | | | --------- 26: 1 = enable, 0 = disable
| | | | ------------ 27: 1 = enable, 0 = disable
| | | | ----------------- 28: 1 = enable, 0 = disable
| | | | --------------------- 29: 1 = enable, 0 = disable
| | | |-------------------------- 30: 1 = enable, 0 = disable
| | | -------------------------- 31: 1 = enable, 0 = disable

Sensor enabled must have been detected as 0x28 (CY17 temperature sensor) during DOW enumeration. This can be verified by using the command 18 (0x12): Read CY17 Temperature Sensors (PCBA Required) (Pg. 37).

The return packet will be:

```
type: 0x40 0x13 = 0x53 = 8310
data_length = 0
```

20 (0x14): Arbitrary DOW Transaction (PCBA Required)

The PLCD-35+PCBA can function as an RS-232 to Dallas1-Wire bridge. PLCD-35+PCBA can send up to 15 bytes and receive up to 14 bytes. This will be sufficient for many devices, but some devices require larger transactions cannot be fully used with the PLCD-35+PCBA. This command allows you to specify arbitrary transactions on the 1-Wire bus. The 1-Wire commands follow this basic layout:
<bus reset> //Required
<address_phase> //Must be "Match ROM" or "Skip ROM"
<write_phase> //optional, but at least one of write_phase or read_phase must be sent
<read_phase> //optional, but at least one of write_phase or read_phase must be sent

type: 0x14 = 20_{10}
valid data_length is 2 to 16
data[0] = device_index (0-32 valid)
data[1] = number_of_bytes_to_read (0-14 valid) 0
data[2-15] = data_to_be_written[data_length-2]

If device_index is 32, then no address phase will be executed. If device_index is in the range of 0 to 31, and a 1-Wire device was detected for that device_index at power on, then the write cycle will be prefixed with a "Match ROM" command and the address information for that device.

If data_length is 2, then no specific write phase will be executed (although address information may be written independently of data_length depending on the value of device_index).

If data_length is greater than 2, then data_length-2 bytes of data_to_be_written will be written to the 1-Wire bus immediately after the address phase.

If number_of_bytes_to_read is 0, then no read phase will be executed. If number_of_bytes_to_read is not 0, then number_of_bytes_to_read will be read from the bus and loaded into the response packet.

The return packet will be:

type: 0x40 | 0x14 = 0x54 = 84_{10}
data_length = 2 to 16
data[0] = device_index (0-31 valid)
data[data_length-2] = Data read from the 1-Wire bus. This is the same as number_of_bytes_to_read from the command.
data[data_length-1] = 1-Wire CRC

21 (0x15): Set Up Live Fan Or Temperature Display (PCBA Required)

You can configure the PLCD-35+PCBA to automatically update a portion of the display with a "live" RPM or temperature reading. Once the display is configured using this command, the PLCD-35+PCBA will continue to display the live reading on the display without host intervention. The Set Up Live Fan or Temperature Display is one of the items stored by command 4 (0x04): Store Current State As Boot State (Pg. 29). You can configure the PLCD-35+PCBA to immediately display fan speeds or system temperatures as soon as power is applied.

The live display is based on a concept of display slots. There are 4 slots. Each of the 4 slots may be enabled or disabled independently.

Any slot may be requested to display any data that is available. For instance, slot 0 could display temperature sensor 3 in °C, while slot 1 could simultaneously display temperature sensor 3 in °F.

Any slot may be positioned at any location on the display, as long as all the digits of that slot fall fully within the display area. It is legal to have the display area of one slot overlap the display area of another slot, but senseless. This situation should be avoided in order to have meaningful information displayed.
type: 0x15 = 21_{10}
Valid data length is 7 or 2 (for turning a slot off)
data[0]: display slot (0-3)
data[1]: type of item to display in this slot
   0 = nothing (data length then must be 2)
   1 = fan tachometer RPM (data length then must be 7)
   2 = temperature (data length then must be 7)
data[2]: index of the sensor to display in this slot:
      0-3 are valid for fans
      0-31 are valid for temperatures (and the temperature sensor must be attached)
data[3]: number of digits
      for a fan: 4 digits (0 to 9999) valid fan speed range
      for a fan: 5 digits (0 to 50000) valid fan speed range
      for a temperature: 3 digits (-XX or XXX)
      for a temperature: 5 digits (-XX.X or XXX.X)
data[4]: display column
      0-13 valid for a 3-digit temperature
      0-12 valid for a 4-digit fan
      0-11 valid for a 5-digit fan or temperature
data[5]: display row (0-1 valid)
data[6]: pulses_per_revolution or temperature units
      for a fan: pulses per revolution for this fan (1 to 32)
      for a temperature: units (0 = deg C, 1 = deg F)

If a 1-Wire CRC error is detected, the temperature will be displayed as "ERR" or "ERROR".

If the frequency of the tachometer signal is below the detectable range, the speed will be displayed as "SLOW" or "STOP".

Displaying a fan tachometer will override the fan power setting to 100% for up to 1/8 of a second every 1/2 second. Please see “Fan Connections” section in the PCBA Datasheet for details.

The return packet will be:
   type: 0x40 | 0x15 = 0x55 = 85_{10}
data_length = 0

22 (0x16): Send Command Directly To The Display Controller

This command allows you to access the PLCD-35's display's controller directly. Note: It is possible to corrupt the PLCD-35 display using this command.

Note
Any command sent specifically to the controller Samsung S6A0073 will need to be reviewed / modified for the commands / registers of the Rockworks RW1067. Please contact us for the RW1067 datasheet.

   type: 0x16 = 22_{10}
data_length: 2
data[0]: location code
      0 = "Data" register
      1 = "Control" register, RE=0
      2 = "Control" register, RE=1
data[1]: data to write to the selected register
The return packet will be:

```
type: 0x40 | 0x16 = 0x56 = 8610
data_length = 0
```

**23 (0x17): Configure Key Reporting**

By default, the PLCD-35 reports any key event to the host. This command allows the key events to be enabled or disabled on an individual basis.

```
#define KP_UL     0x01 //(upper-left)
#define KP_UR     0x02 //(upper-right)
#define KP_LL     0x04 //(lower-left)
#define KP_LR     0x08 //(lower-right)
```

```
type: 0x17 = 2310
data_length = 2
data[0]: press mask
data[1]: release mask
```

Valid values of the mask are \000-\015.

The return packet will be:

```
type: 0x40 | 0x17 = 0x57 = 8710
data_length = 0
```

Configure Key Reporting is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

**24 (0x18): Read Keypad, Polled Mode**

In some situations, it may be convenient for the host to poll the PLCD-35 for key activity. This command allows the host to detect which keys are currently pressed, which keys have been pressed since the last poll, and which keys have been released since the last poll.

This command is independent of the key reporting masks set by command 23 (0x17): Configure Key Reporting (Pg. 41).

```
#define KP_UL     0x01 //(upper-left)
#define KP_UR     0x02 //(upper-right)
#define KP_LL     0x04 //(lower-left)
#define KP_LR     0x08 //(lower-right)
```

```
type: 0x18 = 2410
data_length = 0
```

The return packet will be:

```
type: 0x40 | 0x18 = 0x58 = 8810
data_length = 0
```

**25 (0x19): Set Fan Power Fail-Safe (PCBA Required)**

The PLCD-35+PCBA can be used as part of an active cooling system. The fans can be slowed down to reduce noise when a system is idle or when the ambient temperature is low. The fans can be sped up when the system is under heavy load or the ambient temperature is high.
Since there are a large number of ways to control the speed of the fans (thresholds, thermostat, proportional, PID, multiple temperature sensors contributing to the speed of several fans . . .) there was no way to foresee the particular requirements of your system and include an algorithm in the PLCD-35’s firmware that would be an optimal fit for your application.

Varying fan speeds under host software control gives the ultimate flexibility in system design but would typically have a fatal flaw: a host software or hardware failure could cause the cooling system to fail. If the fans were set at a slow speed when the host software failed, system components may be damaged due to inadequate cooling.

The fan power fail-safe command allows host control of the fans without compromising safety. When the fan control software activates, it should set the fans that are under its control to fail-safe mode with an appropriate timeout value. If for any reason the host fails to update the power of the fans before the timeout expires, the fans previously set to fail-safe mode will be forced to 100% power.

```c
#define FAN_1     0x01
#define FAN_2     0x02
#define FAN_3     0x04
#define FAN_4     0x08

#type = 0x19 = 2510
#data_length = 2
#data[0] = bitmask of fans set to fail-safe (1-15 valid)
#data[1] = timeout value in 1/8 second ticks:
#   1 = 1/8 second
#   2 = 1/4 second
#   255 = 31 7/8 seconds

The return packet will be:

```
#type = 0x40 | 0x19 = 0x59 = 8910
#data_length = 0
```

26 (0x1A): Set Fan Tachometer Glitch Delay (PCBA Required)

The PLCD-35 uses approximately 18 Hz for the PWM repetition rate. The fan’s tachometer output is only valid if power is applied to the fan. Most fans produce a valid tachometer output very quickly after the fan has been turned back on but some fans take time after being turned on before their tachometer output is valid.

This command allows you to set a variable-length delay after the fan has been turned on before the PLCD-35+PCBA will recognize transitions on the tachometer line. The delay is specified in counts, each count being nominally 552.5 µS long (1/100 of one period of the 18 Hz PWM repetition rate).

In practice, most fans will not need the delay to be changed from the default length of 1 count. If a fan’s tachometer output is not stable when its PWM setting is other than 100%, simply increase the delay until the reading is stable. Typically, you would (1) start at a delay count of 50 or 100, (2) reduce it until the problem reappears, and then (3) slightly increase the delay count to give it some margin.

Setting the glitch delay to higher values will make the RPM monitoring slightly more intrusive at low power settings. Also, the higher values will increase the lowest speed that a fan with RPM reporting enabled will “seek” at 0% power setting.

The Fan Glitch Delay is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

```c
#type = 0x1A = 2610
#data_length = 4
#data[0] = delay count of fan 1
#data[1] = delay count of fan 2
#data[2] = delay count of fan 3
#data[3] = delay count of fan 4
```
The return packet will be:

\[
\text{type} = 0x40 \mid 0x1A = 0x5A = 90_{10} \\
data\_length = 0
\]

27 (0x1B): Query Fan Power And Fail-Safe Mask (PCBA Required)

This command can be used to verify the current fan power and verify which fans are set to fail-safe mode.

```c
#define FAN_1     0x01
#define FAN_2     0x02
#define FAN_3     0x04
#define FAN_4     0x08

\text{type} = 0x1B = 27_{10} \\
data\_length = 0
```

The return packet will be:

\[
\text{type} = 0x40 \mid 0x1B = 0x5B = 91_{10} \\
data\_length = 5 \\
data[0] = \text{fan 1 power} \\
data[1] = \text{fan 2 power} \\
data[2] = \text{fan 3 power} \\
data[3] = \text{fan 4 power} \\
data[4] = \text{bitmask of fans with fail-safe set}
\]
28 (0x1C): Set ATX Power Switch Functionality

For ATX CY25, CY38 ATX power cable or the optional PCBA+CY14 ATX power cable is required.

The combination of the PLCD-35 with ATX can be used to replace the function of the power and reset switches in a standard ATX-compatible system. The ATX power switch functionality is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29)

See How to Set ATX Functionality Using the application (Pg. 24) for detailed steps.

Note

The GPIO pins used for ATX control must not be configured as user GPIO. The pins must be configured to their default drive mode in order for the ATX functions to work correctly.

These settings are factory default but may be changed by the user. Please see command 34 (0x22): GPIO Settings (PCBA Required) (Pg. 48). These settings must be saved as the boot state.

To ensure that GPIO[1] will operate correctly as ATX SENSE, user GPIO[1] must be configured as:

DDD = "011: 1=Resistive Pull Up, 0=Fast, Strong Drive Down".
F = "0: Port unused for user GPIO."

This configuration can be assured by sending the following command:

```
command = 34
length = 3
data[0] = 1
data[1] = 0
data[2] = 3
```

To ensure that GPIO[2] will operate correctly as ATX POWER, user GPIO[2] must be configured as:

DDD = "010: Hi-Z, use for input".
F = "0: Port unused for user GPIO."

This configuration can be assured by sending the following command:

```
command = 34
length = 3
data[0] = 2
data[1] = 0
data[2] = 2
```

To ensure that GPIO[3] will operate correctly as ATX RESET, user GPIO[3] must be configured as:

DDD = "010: Hi-Z, use for input".
F = "0: Port unused for user GPIO."

This configuration can be assured by sending the following command:

```
command = 34
length = 3
data[0] = 3
data[1] = 0
data[2] = 2
```

These settings must be saved as the boot state.

The RESET (GPIO[3]) and POWER CONTROL (GPIO[2]) lines on the PLCD-35 with ATX are normally high-impedance. Electrically, they appear to be disconnected or floating. When the PLCD-35 with ATX asserts the RESET or POWER
CONTROL lines, they are momentarily driven high or low (as determined by the AUTO_POLARITY, RESET_INVERT or POWER_INVERT bits, detailed below). To end the power or reset pulse, the PLCD-35 with ATX changes the lines back to high-impedance.

FOUR FUNCTIONS MAY BE ENABLED BY COMMAND 28

Function 1: KEYPAD_RESET
If POWER-ON SENSE (GPIO[1]) is high, holding the upper right key for 4 seconds will pulse RESET (GPIO[3]) pin for 1 second. During the 1-second pulse, the PLCD-35 with ATX will show "RESET", and then reset itself, showing its boot state as if it had just powered on. Once the pulse has finished, the PLCD-35 with ATX will not respond to any commands until after it has reset the host and itself.

Function 2: KEYPAD_POWER_ON
If POWER-ON SENSE (GPIO[1]) is low, pressing the upper right key for 0.25 seconds will pulse POWER CONTROL (GPIO[2]) for the duration specified by in data[1] or the default of 1 second. During this time the PLCD-35 with ATX will show POWER ON, then the PLCD-35 with ATX will reset itself.

Function 3: KEYPAD_POWER_OFF
If POWER-ON SENSE (GPIO[1]) is high, holding the lower right key for 4 seconds will pulse POWER CONTROL (GPIO[2]) for the duration specified by in data[1] or the default of 1 second. If the user continues to hold the power key down, then the PLCD-35 with ATX will continue to drive the line for a maximum of 5 additional seconds. During this time the PLCD-35 with ATX will show "POWER OFF".

Function 4: LCD_OFF_IF_HOST_IS_OFF
If LCD_OFF_IF_HOST_IS_OFF is set, the PLCD-35 with ATX will blank its screen and turn off its backlight to simulate its power being off any time POWER-ON SENSE is low. The PLCD-35 with ATX will still be active (since it is powered by VSB), monitoring the keypad for a power-on keystroke. If +12v remains active (which would not be expected since the host is "off"), the fans will remain on at their previous settings. Once POWER-ON SENSE (GPIO[1]) goes high, the PLCD-35 with ATX will reboot as if power had just been applied to it.

#define AUTO_POLARITY          0x01 //Automatically detects polarity for reset and power (recommended)
define RESET_INVERT           0x02 //Reset pin drives high instead of low (ignored if AUTO_POLARITY is set)
define POWER_INVERT           0x04 //Power pin drives high instead of low (ignored if AUTO_POLARITY is set)
define LCD_OFF_IF_HOST_IS_OFF 0x10
define KEYPAD_RESET           0x20
define KEYPAD_POWER_ON        0x40
define KEYPAD_POWER_OFF       0x80
type: 0x1C = 2810
data_length: 1 or 2
data[0]: bitmask of enabled functions
data[1]: (optional) length of power on & off pulses in 1/32 second
1 = 1/32 sec
2 = 1/16 sec
16 = 1/2 sec
254 = 7.9 seconds
255 = Assert power control line until host power state changes
The return packet will be:

\[
\begin{align*}
\text{type: } & 0x40 | 0x1C = 0x5C = 92_{10} \\
data\_length: & 0
\end{align*}
\]

**29 (0x1D): Enable/Disable And Reset The Watchdog**

Some systems use hardware watchdog timers to ensure that a software or hardware failure does not result in an extended system outage. Once the host system has booted, a system monitor program is started. The system monitor program would enable the watchdog timer on the PLCD-35 with ATX. If the system monitor program fails to reset the watchdog timer, the PLCD-35 with ATX will reset the host system.

\[
\begin{align*}
\text{type: } & 0x1D = 29_{10} \\
data\_length = & 1 \\
data[0] = & \text{enable/timeout}
\end{align*}
\]

If timeout is 0, the watchdog is disabled.

If timeout is 1-255, then this command must be issued again within timeout seconds to avoid a watchdog reset.

To turn the watchdog off once it has been enabled, simply set timeout to 0.

If the command is not re-issued within timeout seconds, then the PLCD-35 with ATX will reset the host (see command 28 (0x1C): Set ATX Power Switch Functionality (Pg. 44) for details). Since the watchdog is off by default when the PLCD-35 powers up, the PLCD-35 with ATX will not issue another host reset until the host has once again enabled the watchdog.

The return packet will be:

\[
\begin{align*}
\text{type: } & 0x40 | 0x1D = 0x5D = 93_{10} \\
data\_length: & 0
\end{align*}
\]

**30: (0x1E) Read Reporting And Status**

This command can be used to verify the current items configured to report to the host, as well as some other miscellaneous status information.

\[
\begin{align*}
\text{type = } & 0x1E = 30_{10} \\
data\_length = & 0
\end{align*}
\]
The return packet will be:

```
<table>
<thead>
<tr>
<th>type</th>
<th>0x40</th>
<th>0x1E = 0x5E</th>
</tr>
</thead>
<tbody>
<tr>
<td>data_length</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>data[0]</td>
<td>fan 1-4 reporting status (as set by command 16)</td>
<td></td>
</tr>
<tr>
<td>data[1]</td>
<td>temperatures 1-8 reporting status (as set by command 19)</td>
<td></td>
</tr>
<tr>
<td>data[2]</td>
<td>temperatures 9-15 reporting status (as set by command 19)</td>
<td></td>
</tr>
<tr>
<td>data[3]</td>
<td>temperatures 16-23 reporting status (as set by command 19)</td>
<td></td>
</tr>
<tr>
<td>data[4]</td>
<td>temperatures 24-32 reporting status (as set by command 19)</td>
<td></td>
</tr>
<tr>
<td>data[5]</td>
<td>key presses (as set by command 23)</td>
<td></td>
</tr>
<tr>
<td>data[6]</td>
<td>key releases (as set by command 23)</td>
<td></td>
</tr>
<tr>
<td>data[7]</td>
<td>ATX Power Switch Functionality (as set by command 28),</td>
<td></td>
</tr>
<tr>
<td>data[8]</td>
<td>current watchdog counter (as set by command 22)</td>
<td></td>
</tr>
<tr>
<td>data[9]</td>
<td>fan RPM glitch delay[0] (as set by command 26)</td>
<td></td>
</tr>
<tr>
<td>data[10]</td>
<td>fan RPM glitch delay[1] (as set by command 26)</td>
<td></td>
</tr>
<tr>
<td>data[12]</td>
<td>fan RPM glitch delay[3] (as set by command 26)</td>
<td></td>
</tr>
<tr>
<td>data[13]</td>
<td>contrast setting (as set by command 13)</td>
<td></td>
</tr>
<tr>
<td>data[14]</td>
<td>backlight setting (as set by command 14)</td>
<td></td>
</tr>
</tbody>
</table>
```

Please Note: Previous and future firmware versions may return fewer or additional bytes.

**31 (0x1F): Send Data To Display**

This command allows data to be placed at any position on the display.

```
<table>
<thead>
<tr>
<th>type</th>
<th>0x1F</th>
<th>31</th>
</tr>
</thead>
<tbody>
<tr>
<td>data_length</td>
<td>3 to 22</td>
<td></td>
</tr>
<tr>
<td>data[0]</td>
<td>col = x = 0 to 19</td>
<td></td>
</tr>
<tr>
<td>data[1]</td>
<td>row = y = 0 to 1</td>
<td></td>
</tr>
<tr>
<td>data[2-21]</td>
<td>text to place on the display, variable from 1 to 20 characters</td>
<td></td>
</tr>
</tbody>
</table>
```

The return packet will be:

```
<table>
<thead>
<tr>
<th>type</th>
<th>0x40</th>
<th>0x1F = 0x5F</th>
</tr>
</thead>
<tbody>
<tr>
<td>data_length</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
```

Send Data to Display is one of the items stored by the command **4 (0x04): Store Current State As Boot State (Pg. 29)**.

**32: Key Legends**

The PLCD-35 offers firmware support for “soft keys”. Eight predefined icons correspond to common key functions:

```
#define KEY_LEGEND_BLANK      0
#define KEY_LEGEND_CANCEL     1
#define KEY_LEGEND_CHECK      2
#define KEY_LEGEND_UP         3
#define KEY_LEGEND_DOWN       4
#define KEY_LEGEND_RIGHT      5
#define KEY_LEGEND_LEFT       6
#define KEY_LEGEND_PLUS       7
#define KEY_LEGEND_MINUS      8
#define KEY_LEGEND_NONE       9 // no key or symbol
```
The host simply enables key legends—specifying the icon to display corresponding to each key—and then the PLCD-35 firmware draws the legends. Each soft-key legend “inverts” when the corresponding hard key is pressed, providing instant feedback that the key has been actuated.

The key legends use special characters 2,3,4,5,6 and 7. Special characters 0 and 1 are available for other functions.

The key legends act as a second layer of the display over the 6 right-most characters. Text written to the key legends area are overwritten instantly by the key legends.

The return packet will be:

```
type: 0x40 | 32
data_length = 0
```

The key reports are not affected by the key legend settings. The host should make the appropriate action based on the key legend settings and the keys reported.

By using special character definitions and key reports, the functionality of the key legends can be emulated in host software, allowing unlimited icon definitions.

Key Legends is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

33 (0x21): Set Baud Rate

After sending this command, the host should wait for a positive acknowledgment from the PLCD-35 at the old baud rate. The host can then begin communicating at the new baud rate.

The baud rate must be saved by command 4 (0x04): Store Current State As Boot State (Pg. 29) if you want the PLCD-35 to power-up/restart using the new baud rate. The factory default baud rate is 115200.

The return packet will be:

```
type: 0x40 | 0x21 = 0x61 = 97
data_length = 0
```

34 (0x22): GPIO Settings (PCBA Required)

The PLCD-35 (hardware versions v2.0 and up, firmware versions 2.0 and up) has five pins for user-definable general purpose input / output (GPIO). These pins are shared with the DOW and ATX functions. Be careful when you configure the GPIO if you want to use the ATX or DOW at the same time.

The architecture of the PLCD-35 allows great flexibility in the configuration of the GPIO pins. They can be set as input or output. They can output constant high or low signals or a variable duty cycle 100 Hz PWM signal.
The default GPIO mode uses PWM and a suitable current limiting resistor to control the LEDs on the front of the display module. They can be turned on and off and even dimmed under host software control. With suitable external circuitry, the GPIOs can also be used to drive external logic or power transistors.

Note
GPIO[1] has R8 (5.6k) in series by default. If you need GPIO[1] to be a low impedance output, please replace R8 with a 0Ω resistor.

The PLCD-35 continuously polls the GPIOs as inputs at 32 Hz. The present level can be queried by the host software at a lower rate. The PLCD-35 also keeps track of whether there were rising or falling edges since the last host query (subject to the resolution of the 32 Hz sampling). This means that the host is not forced to poll quickly in order to detect short events. The algorithm used by the PLCD-35 to read the inputs is inherently "debounced".

The GPIOs also have "pull-up" and "pull-down" modes. These modes can be useful when using the GPIO as an input connected to a switch since no external pull-up or pull-down resistor is needed. For instance, the GPIO can be set to pull up. Then when a switch connected between the GPIO and ground is open, reading the GPIO will return a "1" When the switch is closed, the input will return a "0".

Pull-up/pull-down resistance values are approximately 5kΩ. Do not exceed current of 25 mA per GPIO.

Note
The GPIO pins may also be used for ATX control through the optional PCBA’s 7-pin connector and CY17 temperature sensing through the PCBA’s DOW header. By factory default, the GPIO output setting, function, and drive mode are set correctly to enable operation of the ATX and DOW functions. The GPIO output setting, function, and drive mode must be set to the correct values in order for the ATX function to function properly. The free demonstration software the application may be used to easily check and reset the GPIO configuration to the default state so the ATX and DOW functions will work.

The GPIO configuration is one of the items stored by the command 4 (0x04): Store Current State As Boot State (Pg. 29).

type: 0x22 = 3410
data_length:
2 bytes to change value only
3 bytes to change value and configure function and drive mode
data[0]: index of GPIO to modify on optional PCBA’s connector when using PLCD-35+PCBA+CY14
  0 = GPIO[0] = J8, Pin 7
  1 = GPIO[1] = J8, Pin 6 (default is ATX Host Power Sense)
  2 = GPIO[2] = J8, Pin 5 (default is ATX Host Power Control)
  3 = GPIO[3] = J8, Pin 4 (default is ATX Host Reset Control)
  4 = GPIO[4] = J9, Pin 2 (default is DOW I/O--has 1kΩ hardware pull-up)
  5-255 = not accessible

Please note: Future versions of this command on future hardware display modules may accept additional values for data[0], which would control the state of future additional GPIO pins.

data[1] = Pin output state (actual behavior depends on drive mode): 
  0 = Output set to low 
  1-99 = Output duty cycle percentage (100 Hz nominal) 
  100 = Output set to high 
  101-254 = invalid
data[2] = Pin function select and drive mode (optional, 0-15 valid)

--- FDDD

| | | |-- DDD = Drive Mode (based on output state of 1 or 0)

000: 1=Fast, Strong Drive Up, 0=Resistive Pull Down
001: 1=Fast, Strong Drive Up, 0=Fast, Strong Drive Down
010: Hi-Z, use for input
011: 1=Resistive Pull Up, 0=Fast, Strong Drive Down
100: 1=Slow, Strong Drive Up, 0=Hi-Z
101: 1=Slow, Strong Drive Up, 0=Slow, Strong Drive Down
110: reserved, do not use -- error returned
111: 1=Hi-Z, 0=Slow, Strong Drive Down

----- F = Function

0: Port unused for GPIO. It will take on the default function such as ATX, DOW or unused. The user is responsible for setting the drive to the correct value in order for the default function to work correctly.

1: Port used for GPIO under user control. The user is responsible for setting the drive to the correct value in order for the desired GPIO mode to work correctly.

------ reserved, must be 0

The return packet will be:

type = 0x40 | 0x22 = 0x62 = 9810

data_length = 0

35 (0x23): Read GPIO Pin Levels And Configuration State (PCBA Required)

Please see command 34 (0x22): GPIO Settings (PCBA Required) (Pg. 48) for details on the GPIO architecture.

type: 0x23 = 3510

data_length: 1

data[0]: index of GPIO to query
0 = GPIO[0] = J8, Pin 7
1 = GPIO[1] = J8, Pin 6 (default is ATX Host Power Sense--has series R8 of 5.6kΩ)
2 = GPIO[2] = J8, Pin 5 (default is ATX Host Power Control)
3 = GPIO[3] = J8, Pin 4 (default is ATX Host Reset Control)
4 = GPIO[4] = J9, Pin 2 (default is DOW I/O--has 1KΩ hardware pull-up on PCBA.)
5-255 = not accessible

Please note: Future versions of this command on future hardware display modules may accept additional values for data[0], which would control the state of future additional GPIO pins.
The return packet will be:

type = 0x40 | 0x23 = 0x63 = 9910
data_length = 4

returns:

data[0] = index of GPIO read

data[1] = Pin state & changes since last poll
    ---- -RFS Enable Reporting of this Fan's Tach Input
    | ||| |-- S = state at the last reading
    | ||| |--- F = at least one falling edge has been detected since the last poll
    | ||| |-- R = at least one rising edge has been detected since the last poll
    | |||-- reserved
    (This reading is the actual pin state, which may or may not agree with the pin setting, depending on drive mode and the load presented by external circuitry. Transients that happen between polls will not be detected.)

data[2] = Requested Pin level/PWM level
    0-100: Output duty cycle percentage
    (This value is the requested PWM duty cycle. The actual pin may or may not be toggling in agreement with this value, depending on the drive mode and the load presented by external circuitry.)

data[3] = Pin function select and drive mode
    ---- FDDD
    | |||-- DDD = Drive Mode
    | |----- F = Function
    | |------ reserved, will return 0

<table>
<thead>
<tr>
<th>DDD</th>
<th>Drive Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1=Fast, Strong Drive Up, 0=Resistive Pull Down</td>
</tr>
<tr>
<td>001</td>
<td>1=Fast, Strong Drive Up, 0=Fast, Strong Drive Down</td>
</tr>
<tr>
<td>010</td>
<td>Hi-Z, use for input</td>
</tr>
<tr>
<td>011</td>
<td>1=Resistive Pull Up, 0=Fast, Strong Drive Down</td>
</tr>
<tr>
<td>100</td>
<td>1=Slow, Strong Drive Up, 0=Hi-Z</td>
</tr>
<tr>
<td>101</td>
<td>1=Slow, Strong Drive Up, 0=Slow, Strong Drive Down</td>
</tr>
<tr>
<td>110</td>
<td>reserved</td>
</tr>
<tr>
<td>111</td>
<td>1=Hi-Z, 0=Slow, Strong Drive Down</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>F</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Port unused for GPIO. It will take on the default function such as ATX, DOW or unused. The user is responsible for setting the drive to the correct value in order for the default function to work correctly.</td>
</tr>
<tr>
<td>1</td>
<td>Port used for GPIO under user control. The user is responsible for setting the drive to the correct value in order for the desired GPIO mode to work correctly.</td>
</tr>
<tr>
<td>-----</td>
<td>----------</td>
</tr>
<tr>
<td></td>
<td>reserved, will return 0</td>
</tr>
</tbody>
</table>
CHARACTER GENERATOR ROM (CGROM)

To find the code for a given character, add the two numbers that are shown in bold for its row and column. For example, the superscript “9” is in the column labeled “128d” and in the row labeled “9d”. Add 128 + 9 to get 137. When you send a byte with the value of 137 to the display, then a superscript “9” will be shown.

![Character Generator ROM Table](image)

Figure 11. Character Generated ROM
RELIABILITY AND LONGEVITY

Note: We work to continuously improve our products, including backlights that are brighter and last longer. Slight color variations from display module to display module and batch to batch are normal.

RELIABILITY

<table>
<thead>
<tr>
<th>ITEM</th>
<th>RELIABILITY SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display portion (excluding keypad, status LEDs, and backlights)</td>
<td>50,000 to 100,000 hours</td>
</tr>
<tr>
<td>Keypad</td>
<td>1,000,000 keystrokes</td>
</tr>
<tr>
<td><strong>PLCD-35 white LED display backlight and blue LED keypad backlight</strong></td>
<td><strong>Power-On Hours</strong></td>
</tr>
<tr>
<td></td>
<td>&lt;10,000</td>
</tr>
<tr>
<td></td>
<td>&lt;50,000</td>
</tr>
</tbody>
</table>

Note: For display modules with white LED backlights, adjust backlight brightness so the display is readable but not too bright. Dim or turn off the backlight during periods of inactivity to conserve the white LED backlight lifetime.

Under operating and storage temperature specification limitations, humidity noncondensing RH up to 65%, and no exposure to direct sunlight. Value listed above are approximate and represent typical lifetime.

LONGEVITY (EOL / REPLACEMENT POLICY)

We are committed to making all of our display modules available for as long as possible. For each display module we introduce, we intend to offer it indefinitely. We do not preplan a display module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a display module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue (“End of Life”, EOL) a display module. For example, we must occasionally discontinue a display module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a display module, we will do our best to find an acceptable replacement display module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a “fit, form, and function” replacement display module to the discontinued display module it replaces. However, sometimes a change in component or process for the replacement display module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement display module is still within the stated Data Sheet specifications and tolerances of the discontinued display module, changes may require modification to your circuit and/or firmware. Possible changes include:

- **Backlight LEDs.** Brightness may be affected (perhaps the new LEDs have better efficiency) or the current they draw may change (new LEDs may have a different VF).
- **Controller.** A new controller may require minor changes in your code.
- **Component tolerances.** Display module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a display module whenever possible; we only discontinue a display module if we have no other option. We post Part Change Notices (PCN) on the product’s website page as soon as possible.
CARE AND HANDLING PRECAUTIONS

HANDLING CAUTION: DISPLAY MODULES SHIPPED IN TRAYS
If you receive display modules packed in trays, handle trays carefully by supporting the entire tray. Trays were made to immobilize the display modules inside their packing carton. Trays are not designed to be rigid. Do not carry trays by their edges; trays and display modules may be damaged.

ESD (ELECTROSTATIC DISCHARGE)
The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING
- The exposed surface of the LCD “glass” is actually a polarizer laminated on top of the glass. To protect the polarizer from damage, the display module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the display module, avoid touching the polarizer. Finger oils are difficult to remove.
- Place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the display module, leaving a small gap between the plate and the display surface. We recommend HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the display module.
- Do not modify the six tabs of the metal bezel or make connections to them.
- Solder only to the I/O terminals. Use care when removing solder so you do not damage the PCB. Use care when removing solder so you do not damage the PCB. Use care to keep the exposed terminals clean. Contamination, including fingerprints, may make soldering difficult and the reliability of the soldered connection poor.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the display module.

Caution
Excessive voltage will shorten the life of the display module. You must drive the display within the specified voltage limit. See Absolute Maximum Ratings (Pg. 11).
AVOID SHOCK, IMPACT, TORQUE, OR TENSION

- Do not expose the display module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the display module.
- Do not place weight or pressure on the display module.

CAUTION

All electronics may contain harmful substances. Avoid contamination by using care to avoid damage during handling. If any residues, gases, powders, liquids, or broken fragments come in contact with your skin, eyes, mouth, or lungs, immediately contact your local poison control or emergency medical center.

HOW TO CLEAN

1. Turn display module off.
2. Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”).
3. If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.
4. If you must clean with a liquid, never use glass cleaners, as they may contain ammonia or alcohol that will damage the polarizer over time. Never apply liquids directly on the polarizer. Long contact with moisture may permanently spot or stain the polarizer. Use filtered water to slightly moisten a clean lint-free microfiber cloth designed for cleaning optics. (For example, use a cloth sold for cleaning plastic eyeglasses.)
5. The plastic is easily scratched or damaged. Use a light touch as you clean the polarizer. Wipe gently.
6. Use a dry microfiber cloth to remove any trace of moisture before turning on the display module.
7. Gently wash the microfiber cloths in warm, soapy water and air dry before reuse.

OPERATION

- Your circuit should be designed to protect the display module from ESD and power supply transients.
- Observe the operating temperature limitations: a minimum of 0°C to a maximum of +50°C with minimal fluctuation. Operation outside of these limits may shorten life and/or harm display. Changes in temperature can result in changes in contrast.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.
- For display modules with white LEDs (CFA631-TMF-KU and CFA631P-TMF-KU), adjust backlight brightness so the display is readable but not too bright. Dim or turn off the backlight during periods of inactivity to conserve the white LED backlight lifetime.

STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight, fluorescent lamps, or any ultraviolet ray with humidity less than 90% noncondensing.
- Observe the storage temperature limitations: -10°C minimum, +60°C maximum with minimal fluctuation. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the display modules while they are in storage.
- To discard, please recycle your display modules at an approved facility.
APPENDIX A: QUALITY ASSURANCE STANDARDS

INSPECTION CONDITIONS

- Environment
  - Temperature: 25±5°C
  - Humidity: 30~85% RH
- For visual inspection of active display area
  - Source lighting: two 20 watt or one 40 watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance: 30±5 cm (about 12 inches)
  - Viewing angle: inspect at 45° angle of normal line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our modules as accurately as possible. For the photos, we adjust for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.
DEFINITION OF ACTIVE AREA AND VIEWING AREA

ACCEPTANCE SAMPLING

<table>
<thead>
<tr>
<th>DEFECT TYPE</th>
<th>AQL*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Major</td>
<td>≤0.65%</td>
</tr>
<tr>
<td>Minor</td>
<td>&lt;1.0%</td>
</tr>
</tbody>
</table>

*AQL* Acceptable Quality Level: maximum allowable error rate or variation from standard

DEFECTS CLASSIFICATION

Defects are defined as:

- A **major defect** is a defect that substantially reduces usability of unit for its intended purpose.
- A **minor defect**: is a defect that is unlikely to reduce usability for its intended purpose.
# ACCEPTANCE STANDARDS

<table>
<thead>
<tr>
<th>#</th>
<th>DEFECT TYPE</th>
<th>ACCEPTANCE STANDARDS CRITERIA</th>
<th>MAJOR / MINOR</th>
</tr>
</thead>
</table>
| 1 | Electrical defects                                               | 1. No display, display malfunctions, or shorted segments.  
2. Current consumption exceeds specifications.                                      | Major         |
<p>| 2 | Viewing area defect                                              | Viewing area does not meet specifications. (See Inspection Conditions (Pg. 56).                     | Major         |
| 3 | Contrast adjustment defect                                       | Contrast adjustment fails or malfunctions.                                                      | Major         |
| 4 | Blemishes or foreign matter on display segments                   | Defect Size (mm) | Acceptable Qty |
|   |                                                                   | ≤0.3 | 3 |
|   |                                                                   | ≤2 defects within 10 mm of each other                                                              | Minor         |
| 5 | Other blemishes or foreign matter outside of display segments     | Defect size = (A + B)/2                                                                         | Minor         |
|   |                                                                   | ≤0.15 | Ignore |
|   |                                                                   | 0.15 to 0.20 | 3 |
|   |                                                                   | 0.20 to 0.25 | 2 |
|   |                                                                   | 0.25 to 0.30 | 1 |
| 6 | Dark lines or scratches in display area                           | Defect Width (mm) | Defect Length (mm) | Acceptable Qty |
|   |                                                                   | ≤0.03 | ≤3.0 | 3 |
|   |                                                                   | 0.03 to 0.05 | ≤2.0 | 2 |
|   |                                                                   | 0.05 to 0.08 | ≤2.0 | 1 |
|   |                                                                   | 0.08 to 0.10 | ≤3.0 | 0 |
|   |                                                                   | ≥0.10 | &gt;3.0 | 0 |
| 7 | Bubbles between polarizer film and glass                          | Defect Size (mm) | Acceptable Qty |
|   |                                                                   | ≤0.20 | Ignore |
|   |                                                                   | 0.20 to 0.40 | 3 |
|   |                                                                   | 0.40 to 0.60 | 2 |
|   |                                                                   | ≥0.60 | 0 |</p>
<table>
<thead>
<tr>
<th>#</th>
<th>DEFECT TYPE</th>
<th>ACCEPTANCE STANDARDS CRITERIA (Continued)</th>
<th>MAJOR / MINOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>Display pattern defect</td>
<td><img src="image" alt="Diagram" /></td>
<td>Minor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{(A+B)}{2} \leq 0.2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C &gt; 0$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{(D+E)}{2} \leq 0.25$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{(F+G)}{2} \leq 0.25$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Acceptable Qty</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\leq 3$ total defects</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\leq 2$ pinholes per digit</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Backlight defects</td>
<td>1. Light fails or flickers.*</td>
<td>Minor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Color and luminance do not correspond to specifications.*</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>3. Exceeds standards for display’s blemishes or foreign matter (see test 5, Pg. 58), and dark lines or scratches (see test 6, Pg. 58).</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>*Minor if display functions correctly. Major if the display fails.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>COB defects</td>
<td>1. Pinholes $&gt;0.2$ mm.</td>
<td>Minor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Seal surface has pinholes through to the IC.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. More than 3 locations of sealant beyond 2 mm of the sealed areas.</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>PCB defects</td>
<td>1. Oxidation or contamination on connectors.*</td>
<td>Minor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Wrong parts, missing parts, or parts not in specification.*</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>*Minor if display functions correctly. Major if the display fails.</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Soldering defects</td>
<td>1. Unmelted solder paste.</td>
<td>Minor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Cold solder joints, missing solder connections, or oxidation.*</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Solder bridges causing short circuits.*</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Solder balls.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>*Minor if display functions correctly. Major if the display fails.</td>
<td></td>
</tr>
</tbody>
</table>